Shri S.V.M. Institute of Technology, Bharuch

Electronics & Telecommunication Department

Mid-Semester Examination Syllabus

Testing & Verification (2181107)

B.E. 4th (8th Semester) (ETC)

Name of faculty: Prof.N.N.Parmar

Chapter No.	Topic
1	**Introduction:**
	Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.
2	**Design & Testability:**
	Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability
3	**Logic and Fault Simulation:**
	Introduction, Simulation Models, Logic Simulation, Fault Simulation

Text Book:

1. VLSI Test Principles and Architectures: Design for Testability,
   Wang Wu Wen, Morgan Kaufmann Publishers